REMARKS

Amendments to the Drawings

Drawing Objections under U.S.C. § 1.84(p)(5)

The drawings were objected to under 37 U.S.C. § 1.84(p)(5). The Examiner noted that while Figure 2 was described in the text, Figures 2A and 2B were not. The Examiner also noted that Figure 15 was not described in the text, and that Figures 15 and 32, had reference signs (elements 210 and 220 in Figure 15 and element 340 in Figure 32) that are not mentioned in the description.

Applicant has amended the specification to change the references to Figure 2 to Figures 2A and 2B. The specification was also amended to describe element 340, the control circuit, of Figure 32. Further, the specification was amended to describe Figure 15 and the references 210 and 220.

Applicant submits that these amendments do not constitute new matter because of the following reasons: Figures 2A and 2B resulted when Figure 2 of the originally filed parent application was divided into 2 views in preparation of the formal drawings and therefore Figures 2A and 2B and their amended description in paragraphs [0017] and [0067] contain no new matter. Figure 15 was described in the Figure itself and in the text at paragraph [0030] and thus the amendment of the specification at paragraph [0102] to describe Figure 15 does not constitute new matter. The reference numbers 210 and 220 of Figure 15 refer to blocks 0 and 15 and therefore amendment of paragraph [0132] referring to blocks 0 and 15 of a memory device does not constitute new matter. Element 340 is shown in Figure 32 as a control circuit, and referred to in paragraph [0140] as a control circuit of the synchronous memory 300, and thus the amendment of paragraph [0140] to refer to control circuit 340 and correct the typographical error does not constitute new matter.

The Applicant respectfully submits that the proposed changes to the description for Figures 2A, 2B, 15, and 32 do not comprise new matter and that the requirements of 37 U.S.C. § 1.84(p)(5) for Figures 2A, 2B, 15 and 32 are satisfied. Applicant therefore requests that the objection under 37 U.S.C. § 1.84(p)(5) be withdrawn.

Amendments to the Specification

The specification was amended to clarify the issues identified in reference to the drawings under 37 U.S.C. § 1.84(p)(5) by the Examiner.

Specifically, the specification was amended at paragraphs [0017] and [0067] to change the references to Figure 2 to Figures 2A and 2B. The specification was also amended at paragraph [0102] to describe element 340, the control circuit, of Figure 32. The specification was further amended at paragraph [0140] and [0132] to describe Figure 15.

As detailed above, Applicant submits that these amendments do not constitute new matter and the Applicant therefore respectfully requests approval of the amendments to the specification.

Amendments to the Claims

Claims 21 and 24 are herein amended.

Claim Rejections Under 35 U.S.C. § 112

Claims 12-14 and 21-24 were rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement. The Examiner stated that the claims contain subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Applicant respectfully traverses the rejection.

The Examiner maintained, in regard to claims 12-14, that "[t]he method of command interleaving in a synchronous memory device" and, in regard to claims 21-24, that "the method of operating a synchronous memory device" were not described in the specification.

From this, Applicant is unsure as to which features of claims 12-14 and 21-24 the Examiner asserts were not described in the specification and requests that the Examiner give a full explanation of which specific elements in claims 12-14 and 21-24 were considered not to be described in the specification, as required under MPEP §706.03(c) and §2164.04.

Applicant maintains that claims 12-14 and 21-24 are supported, at least, by Figures 9, 12 and 30-31 and by paragraphs [0136]-[0146] on pages 40-43 of the specification.

Claim 12 recites a method of command interleaving in a synchronous memory device comprising receiving a read command to initiate a read operation, and receiving a write command sequence during a wait period of the read operation or concurrently with output of data from the read command. Paragraph [0138] on pages 40-41 states, in part,

> "The synchronous Flash memory provides for a latency free write operation. This is different from a SDRAM that requires the system to provide latency for write operations, just like a read operation. So the write operation does not take away from the system bus as many cycles as the SDRAM takes, and hence can improve the system read throughput, see Figure 12 where the write data, Din, is provided on the same clock cycle as the write command and column address. The clock cycle, T1, of Figure 12 does not need to be a NOP command (see Figure 30). The read command can be provided on the next clock cycle following the write data. Thus, while the read operation requires that the DQ connections remain available for a predetermined number of clock cycles following the read command (latency), the DQ connections can be used immediately after the write command is provided (no latency). As such, the present invention allows for zero bus turn around capability. This is substantially different from the SDRAM, where multiple waits are required on the system bus when going between read and write operations."

Paragraphs [0143] and [0144] on page 42 state,

> "In one embodiment, a method of writing to a synchronous memory device is provided. The method comprises providing a write command and write data from a processor to the synchronous memory device on a first clock cycle. The write data is then stored in a write latch of the synchronous memory device, and a write operation is performed to copy the write data from the write latch to a memory array of the synchronous memory device. Finally, a read command is communicated from the processor to the synchronous memory device on a second clock cycle immediately following the first clock cycle to initiate a read operation on the memory array." and

> "The present invention can also eliminate clock, or CAS, latency between read and subsequent write operations. Referring to Figure 9, the LCR command (40H) is provided on clock cycle T1 immediately following the read column cycle (T0). As explained, the write operation command sequence includes at least three clock cycles: an LCR cycle, an active/row cycle, and a write/column cycle. Depending upon the latency of the read operation, one or more NOP clock cycles may be provided to avoid bus contention. The preset invention, therefore, does not require latency between the read column command cycle and the LCR write cycle. The present invention, therefore, provides for more efficient data bus utilization by allowing for read-to-write without latency, and write-to-read without clock cycle delays."

Claim 21, as amended, recites a method of operating a synchronous memory device comprising executing a write operation from an internal write latch on a first part of a memory

array of the synchronous memory device while executing a read operation on a second part of the memory array. Paragraphs [0136] and [0137] on page 40, state, in part,

> "Referring to Figure 30, the timing of a write operation followed by a read to a different bank is illustrated. In this operation, a write is performed to bank a and a subsequent read is performed to bank b. The same row is accessed in each bank." and
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> "Referring to Figure 31, the timing of a write operation followed by a read to the same bank is illustrated. In this operation, a write is performed to bank a and a subsequent read is performed to bank a. A different row is accessed for the read operation, and the memory must wait for the prior write operation to be completed. This is different from the read of Figure 30 where the read was not delayed due to the write operation."

Paragraph [0139] on page 41 states, in part,

> "Referring to Figure 32, a system 300 of the present invention includes a synchronous memory 302 that has internal write latches 304 that are used to store write data received on the DQ inputs 306. The write latches are coupled to the memory array 310. Again, the memory array can be arranged in a number of addressable blocks. Data can be written to one block while a read operation can be performed on the other blocks. The memory cells of the array can be non-volatile memory cells."

Applicant contends that relevant features of claims 12 and 24 have been described in the specification to allow one skilled in the art to practice the invention. As claims 13-14 and 22-24 depend from and further define claims 12 and 21, respectively, they are also considered to be enabled by the specification.

The Applicant therefore requests that the rejection of claims 12-14 and 21-24 under 35 U.S.C. § 112, first paragraph, be withdrawn in that the specification does clearly describe the invention in a way to enable one skilled in the art to make or use the invention.

Double Patenting Rejection

Claims 1-11 and 15-24 were rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-27 of U.S. Patent No. 6,728,161. Included with the present Response, Applicant has attached a Terminal Disclaimer complying with 37 CFR §3.73(b) in response the Examiner's rejection.

Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under the judicially created doctrine of obviousness-type double patenting and allowance of claims 1-11 and 15-24.

Claim Rejections Under 35 U.S.C. § 103

Claims 6-11 and 15-20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Patel (U.S. Patent No. 5,539,696). Applicant respectfully traverses this rejection and requests reconsideration of the claims. Applicant submits that claims 6-11 and 15-20 are allowable for the following reasons.

The Examiner stated, in part, that Patel disclosed a synchronous memory wherein "each of memory bank sections can be separately independently accessed (see lines 64-67, column 5 by accessing alternatively between memory banks with a delay associated with (see lines 65-67, column 7 and lines 1-6, column 8)." Applicant disagrees and maintains that Patel teaches a synchronous memory device that allows faster overall burst read and write operations of the synchronous memory device by using parallel latches, wherein each latch is coupled to an independent column section of a single array bank. Applicant therefore maintains that Patel does not teach or suggest memory banks that are independently accessible for separate read and/or write operations but column sections within a single bank. *See, e.g.*, Patel, column 5, line 53 to column 6, line 1 and column 6, lines 14-27. Applicant has also carefully reviewed Patel and has found no mention of simultaneous execution of a write operation while executing a read operation in the memory array of Patel. In this review, Applicant has also not found any mention in Patel of the synchronous memory receiving at its interface a read command immediately following a write command or a write command interleaved in a read command as described by the present invention. As such, Applicant submits that the memory disclosed in Patel can only execute a single read and write operation at a time and executes single burst read or write operations on a single bank that has multiple column independent sections wherein each column independent section is accessed sequentially so that the overall memory device can operate at a higher speed while allowing the independent column sections to operate at a lower speed. *See, e.g.*, column 5, lines 32-43, and column 7, line 50 to column 8, line 2.

Applicant therefore respectfully submits that Patel does not teach or suggest a synchronous memory device with a memory array with independently accessible memory banks, wherein read and write operations can be simultaneously executed on separate memory banks, as maintained by the Examiner. The Applicant also respectfully submits that Patel does not teach

or disclose a synchronous memory device that can receive at its interface a read command immediately following a write command or a write command interleaved in a read command, as maintained by the Examiner.

In addition to the above arguments regarding Patel not teaching or suggesting synchronous memory device with a memory array with independently accessible memory banks, wherein read and write operations can be simultaneously executed on separate memory banks or a synchronous memory device that can receive at its interface a read command immediately following a write command or a write command interleaved in a read command, Applicant further contends that there is no motivation or suggestion to modify the reference in this manner. Specifically, Applicant contends that to modify Patel to provide simultaneously executed read and write operations on separate memory banks or a synchronous memory device that can receive at its interface a read command immediately following a write command or a write command interleaved in a read command would require a modification of Patel's read/write circuitry to allow the latching of write data and writing to a first bank of a memory array while reading from two or more remaining banks of the memory array. Patel expressly teaches away from simultaneous read and write operations on separate banks and also from interleaved read and write commands on its interface. As stated above, while single burst read or write operations may be executed in parallel in each of the independent column sections of a single memory array bank, the synchronous memory of Patel is restricted to executing a single read or write operation at a given time period. *See, e.g.*, Patel, column 5, line 53 to column 6, line 1, column 6, lines 14-27, column 5, lines 32-43, and column 7, line 50 to column 8, line 2.

Applicant also finds no motivation or suggestion to modify the operation of Patel expressly or impliedly contained in the Patel reference, and the Office Action does not provide a convincing line of reasoning as to why an artisan would have found the claimed invention to have been obvious in light of the teachings of the reference.

Applicant thus submits that the Office has also failed to meet its burden of establishing a *prima facie* case of obviousness. *See* MPEP § 706.02(j) ("The initial burden is on the examiner to provide some suggestion of the desirability of doing what the inventor has done. 'To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must

present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references.'").

Claim 6 recites, in part, "receiving write data on a first clock cycle, storing the write data and executing a data write operation, and executing a data read operation on a next clock cycle immediately following the first clock cycle." As detailed above, Applicant submits that Patel fails to teach or suggest such a memory device or receiving and executing a read command immediately following a write command. As such, Patel fails to teach or suggest all elements of independent claim 6.

Claim 15 recites, in part, "providing a first command of a write command sequence across the synchronous memory bus to the synchronous memory device on a second clock cycle immediately following the first clock cycle to initiate a write operation such that the write command is provided prior to or concurrently with providing output read data from the read operation on an external data connection of the synchronous memory device." As detailed above, Applicant submits that Patel fails to teach or suggest such a system or interleaving a write command with a read command to a synchronous memory device. As such, Patel fails to teach or suggest all elements of independent claim 15.

Claim 18 recites, in part, "providing write data across a synchronous memory bus to the synchronous memory device on a first clock cycle of the synchronous memory bus, and providing a read command across the synchronous memory bus to the synchronous memory device on a second clock cycle immediately following the first clock cycle to initiate a read operation." As detailed above, Applicant submits that Patel fails to teach or suggest such a system or a synchronous memory device receiving and executing a read command immediately following a write command. As such, Patel fails to teach or suggest all elements of independent claim 18.

Applicant respectfully contends that the Examiner has not met the burden of establishing a *prima facie* case of obviousness in regards to claims 6, 15 and 18, and, in addition, that claims 6, 15 and 18 as pending have been shown to be patentably distinct from the cited reference, either alone or in combination with the Examiner's taking of official notice. As claims 7-11, 16-17, and 19-20 depend from and further define claims 6, 15 and 18, respectively, they are also believed to be allowable. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claims 6-12 and 15-20.

Claim Rejections Under 35 U.S.C. § 102

Claims 12-14 were rejected under 35 U.S.C. § 102(e) as being anticipated by Li (U.S. Patent No. 6,154,418). Applicant respectfully traverses this rejection and reserves the right to swear behind the cited reference. The Applicant submits that claims 12-14 are allowable for at least the following reasons.

Claim 12 recites, "a method of command interleaving in a synchronous memory device comprising receiving a read command to initiate a read operation, and receiving a write command sequence during a wait period of the read operation or concurrently with output of data from the read command." Applicant respectfully maintains that Li teaches a double data rate synchronous DRAM (DRR-SDRAM) memory device which splits each memory array bank into two separately accessible planes and, to overcome system clock/DQS latency issues, receives a first and second data on separate data strobes, aligns the first and second data with a first clock signal and writes the aligned data to the two separate planes of the memory array. Applicant submits that, contrary to the Examiner's assertion, Li discloses data interleaving from a single write command to the two separate data planes of each array bank, and not interleaving of read and write commands. *See, e.g.*, Li, claim 1, column 1, lines 34-67, column 2 lines 11-23, and column 5 lines 16-35, 47-63.

Applicant therefore respectfully submits that Li does not teach or disclose a synchronous memory device with command interleaving of read and write commands, as maintained by the Examiner. Applicant further submits that Li fails to teach or disclose such a synchronous memory device receiving a read command to initiate a read operation, and receiving a write command sequence during a wait period of the read operation or concurrently with output of data from the read command. As such, Li fails to teach or disclose all elements of independent claim 12.

As claims 13-14 depend from and further define claim 12, they are also considered to be in condition for allowance. Accordingly, Applicant respectfully requests withdrawal of the rejection under 35 U.S.C. § 102(b) and allowance of claims 12-14.

Claims 21-24, were rejected under 35 U.S.C. § 102(a) as being anticipated by Thummalapally et al. (U.S. Patent No. 6,016,270). Applicant respectfully traverses this rejection and submits that claims 21-24 are allowable for at least the following reasons.

Applicant's claim 21, as amended, recites, "a method of operating a synchronous memory device comprising executing a write operation from an internal write latch on a first part of a memory array of the synchronous memory device while executing a read operation on a second part of the memory array." Applicant respectfully maintains that Thummalapally et al. teaches an asynchronous flash memory device that allows time sharing of an internal bus through use of local row and column address latches coupled to separate banks to internally interleave read and algorithmic operations. The Applicant notes that the differences in synchronous memory and asynchronous memory are well known in the art and therefore maintains that a person of ordinary skill in the art would not recognize the asynchronous flash memory device of Thummalapally et al. as a synchronous memory device. Applicant further notes that Thummalapally et al.'s local row and column latches do not correspond to Applicant's write data latches as Thummalapally et al.'s local row and column latches store the input row and column address for the selected bank, allowing the internal bus to be released for other operations. The local row and column latches do not store the data to be written. *See, e.g.*, Thummalapally et al., Figure 2, column 4, lines 51-67, and column 5, line 1-23. Applicant therefore respectfully submits that Thummalapally et al. does not teach or disclose a synchronous memory device that can execute a write operation from an internal write latch on a first part of a memory array of the synchronous memory device while executing a read operation on a second part of the memory array. As such, Thummalapally et al. fails to teach or disclose all elements of independent claim 21.

As claims 22-24 depend from and further define claim 12, they are also considered to be in condition for allowance. Accordingly, Applicant respectfully requests withdrawal of the rejection under 35 U.S.C. § 102(b) and allowance of claims 21-24.

CONCLUSION

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2207.

Respectfully submitted,

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